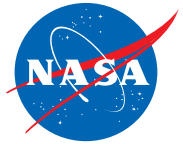


Processing and Prolonged 500 °C Testing of 4H-SiC JFET Integrated Circuits with Two Levels of Metal Interconnect

David J. Spry[1], Philip G. Neudeck[1], Liangyu Chen[2], Dorothy Lukco[3], Carl W. Chang[3], Glenn M. Beheim[1], Michael J. Krasowski[1], and Norman F. Prokop[1]

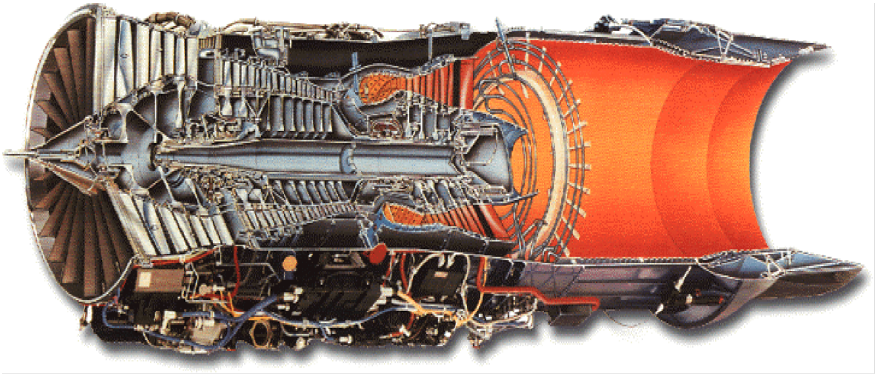
[1]NASA Glenn Research Center

[2]Ohio Aerospace Institute

[3]Vantage Partners LLC

SiC Electronics Benefits to NASA Missions

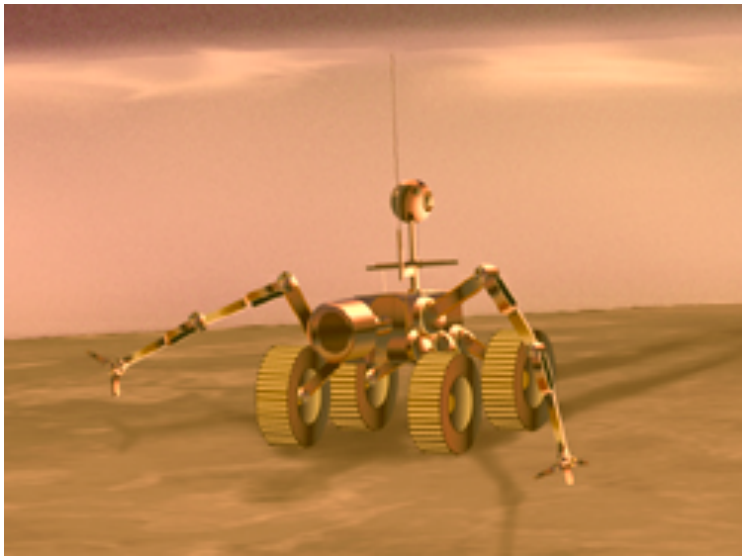
Intelligent Propulsion Systems



"GEER" Venus Test Chamber

Hybrid Electric Aircraft

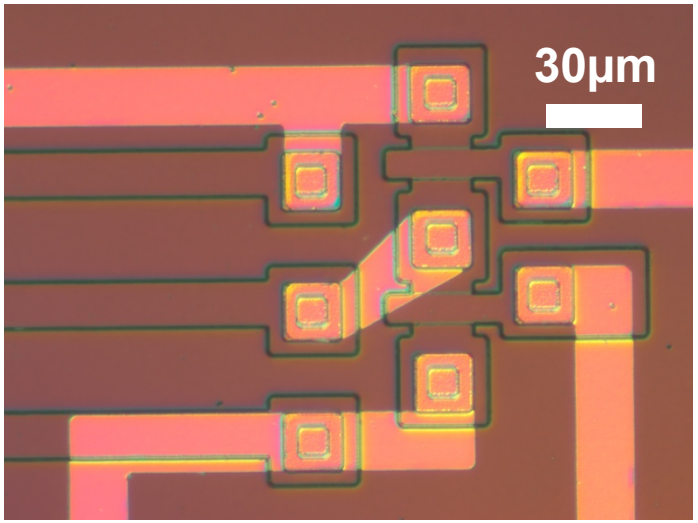
Venus Exploration

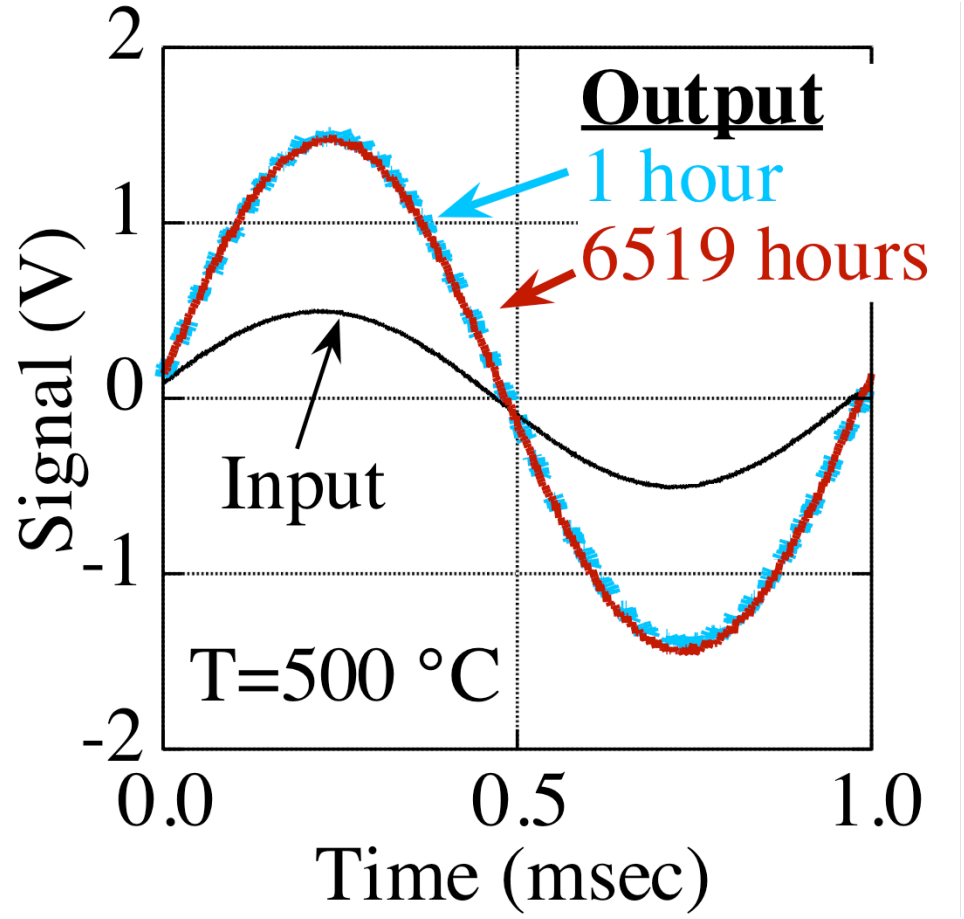


NASA GRC's internal research effort has been to focus on durable integrated circuits at 500 °C for > 3000 hrs.

Past work with single layer of interconnect

- Differential amplifier made in 6H-SiC operated 6519 hours at 500 °C in air ambient[1].
- Complexity limited. Only 2 transistors and 3 resistors.
- JFET approach good for minimizing gate leakage at 500 °C.





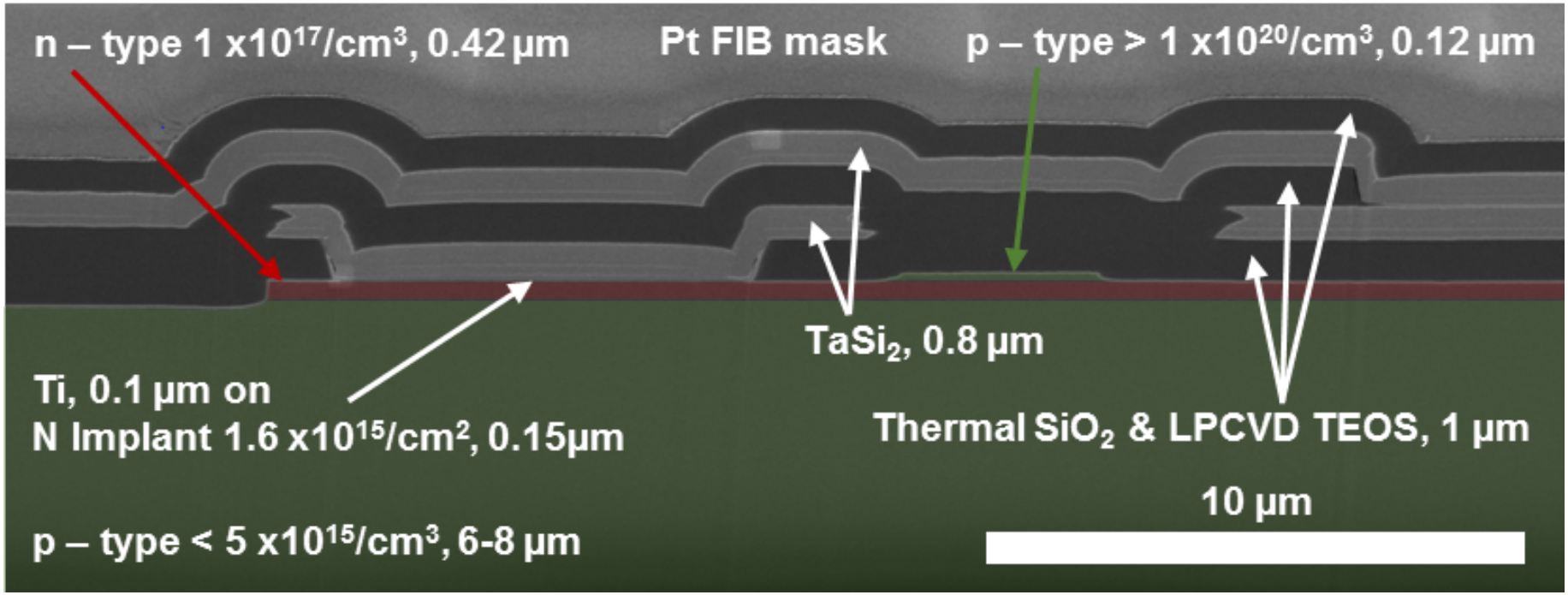
[1] Phys. Status Solidi A **206**, No. 10, 2329–2345 (2009)

Two levels of metal interconnect

Processing enhancements for conformal processing on topology.

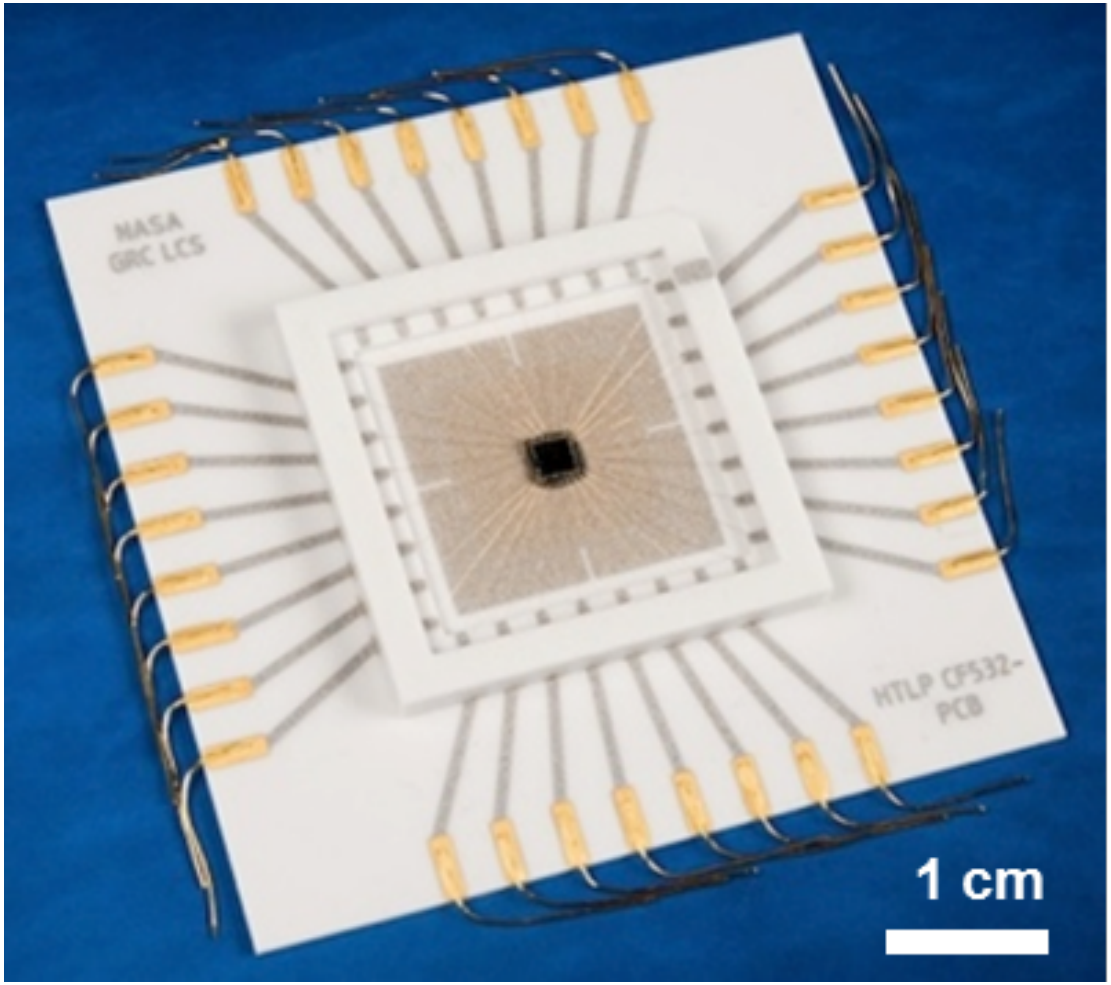
- Proximity sputtering of $TaSi_2$ (21mm target to substrate spacing).
- LPCVD tetraethyl orthosilicate (TEOS) deposited 720 °C.
- Design rules for thick dielectrics and metal traces.

Enables crisscrossing traces and on chip capacitors. Now 4H-SiC JFET



New high-T packaging (32 pins)

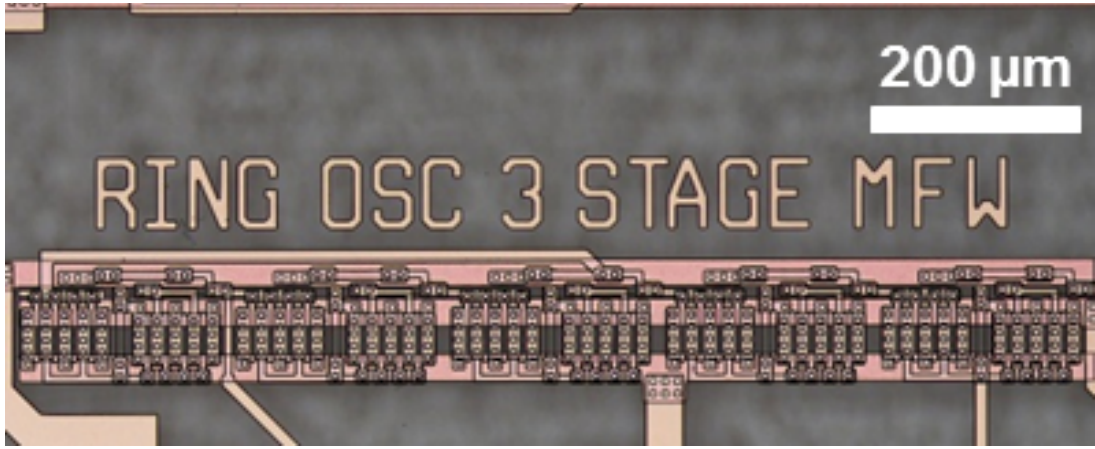
- A new 32 pin package and circuit board was developed by Dr. Liangyu Chen for testing.
- Devices were tested without lid in air ambient at 500 °C (as seen in photo).
- 13 chips high-T package tested to date.
- Hundreds of die wafer probed at RT.



Logic gates – 500 °C test results

- **A 3 stage ring oscillator (shown at right) lasted over 3000 hours at 500 °C.**
- Differences in lifetime most likely due to processing non-idealities discussed in a separate paper at this conference [2].

(10 transistors and 15 resistors)

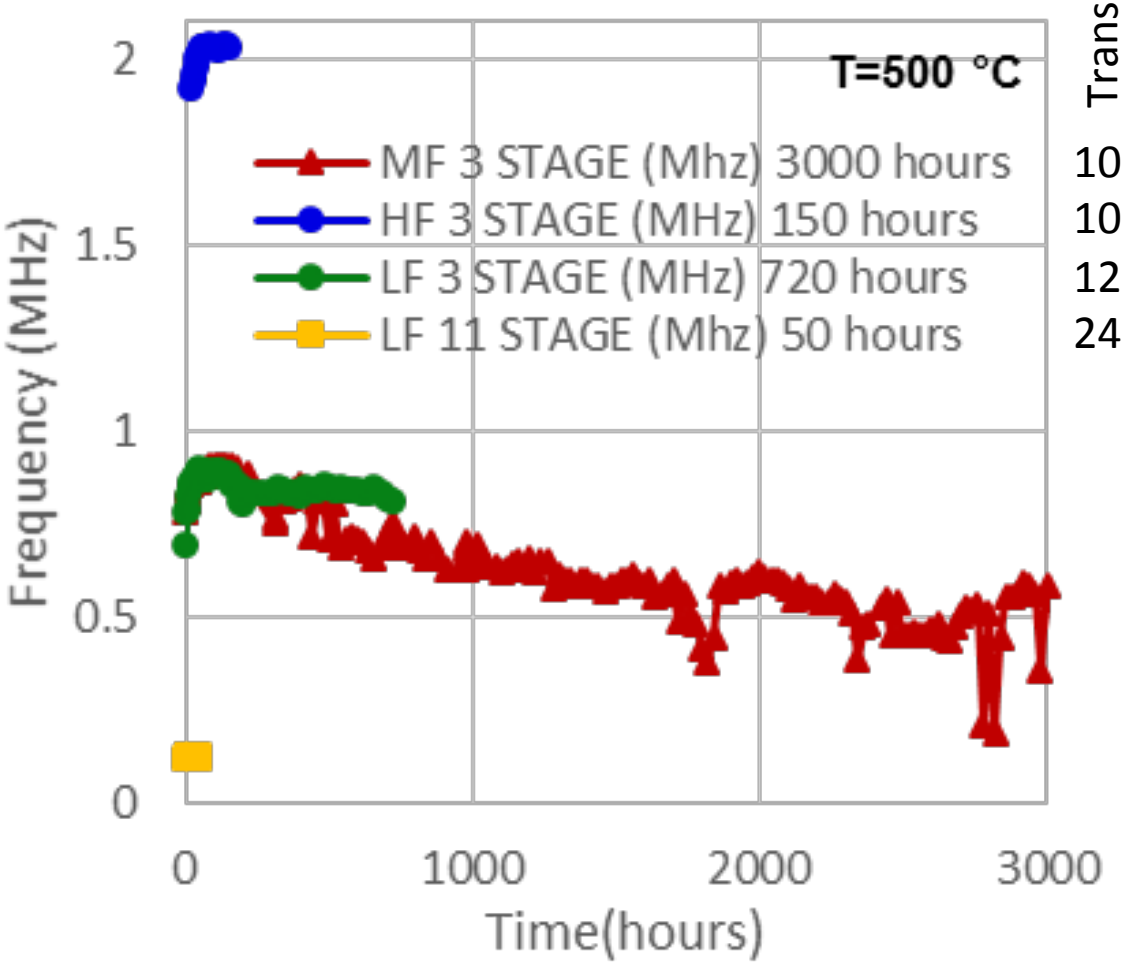


- Two individual NOT circuits of different designs functioned 1160 hours and 2720 hours at 500 °C.
- AND and NOR gates functioned 220 hours and 240 hours at 500 °C, respectively.
- Separate set of NOT, NAND, and NOR circuit tied to a common input failed after 25 hours at 500 °C.

[2] Evidence of Processing Non-Idealities in 4H-SiC Integrated Circuits Fabricated With Two Levels of Metal Interconnect. Monday ICSCRM2015 Poster

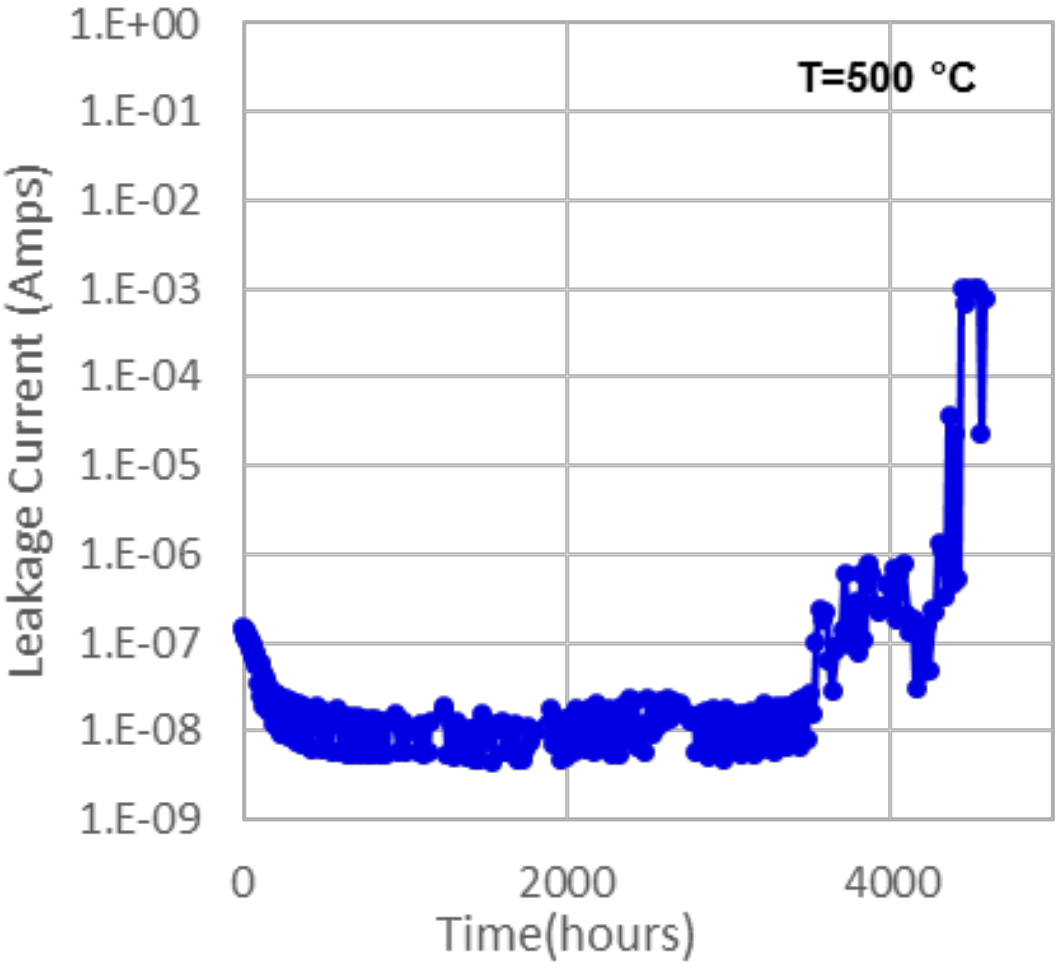
Ring oscillators – 500 °C results

- 500 °C testing of four different designs of oscillators.
- Two fail in less than 200 hours.



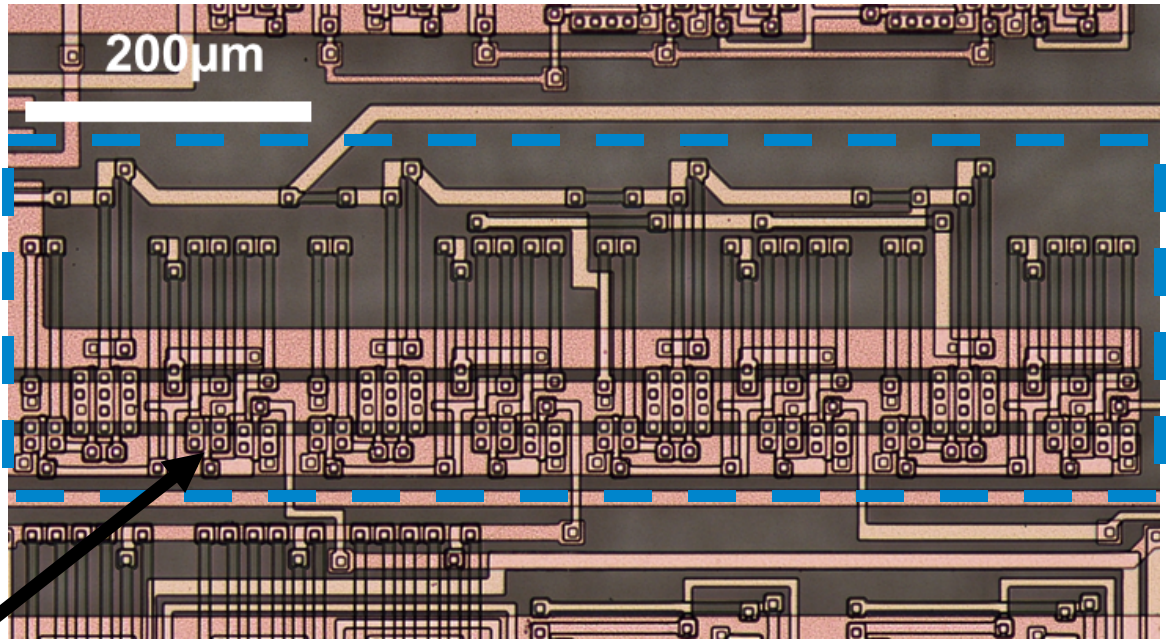
On chip capacitor - test results

- Leakage current of a 15 pf capacitor with an area of 0.5mm^2.
- 500 °C Durability testing was 50% duty cycle 50V/ 0V with 20 hour stress cycles.
- Classic bathtub curve shape, but is really burn and failure.



D to A (4-Bit) IC

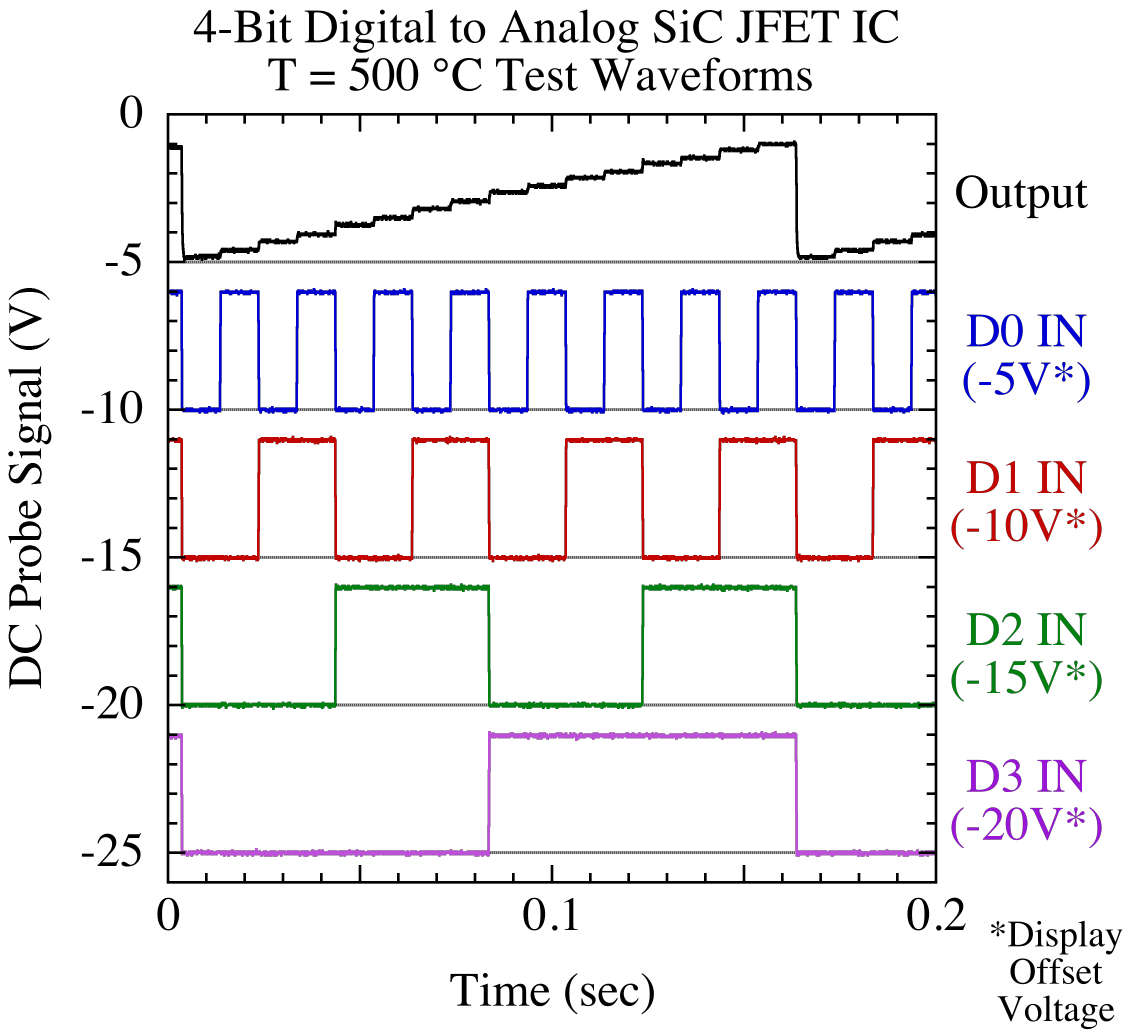
- Even more complex circuits than the ring oscillators worked at 500 °C, but with lower room temperature yields and 500 °C durability.
- D to A was part of a larger A to D IC, but mask layout error caused other sections not to working.
- The two layer interconnects allows for simpler and denser routing with VSS, VDD, and GND bus lines.



4-Bit Digital to Analog
(20 Transistors)

D to A (4-bit) IC

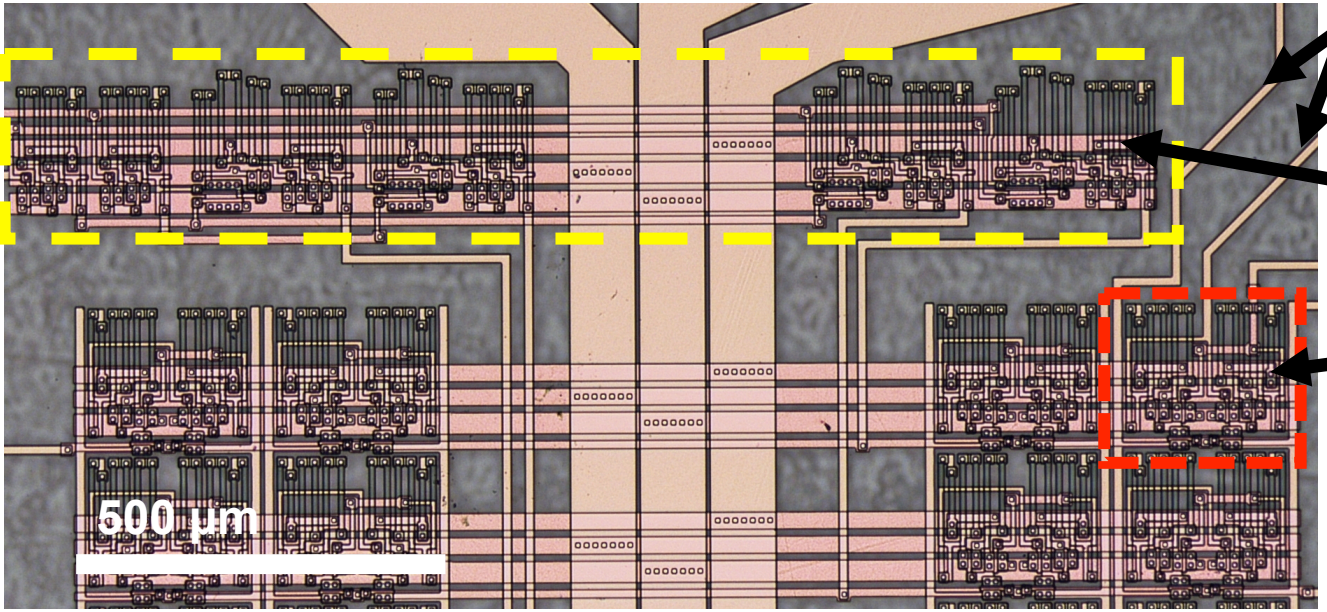
- D to A operated for 10 hours at 500 °C.
- Note: normally on 4H-SiC JFETs ICs are designed for negative voltage logic signals.



-1 V to -5 V logic

Address Decoder and RAM ICs

- Both were part of 4x4 (16 bit) test memory IC, but sodium contamination prevented read amplifiers from working at high-T.
- Note: VSS, VDD, and GND have vertical and horizontal bus lines. The vertical bus lines were not permitted over device area and had multiple bond pads on both sides of the die.
- Note: the gray speckle in the field is the backside contact.



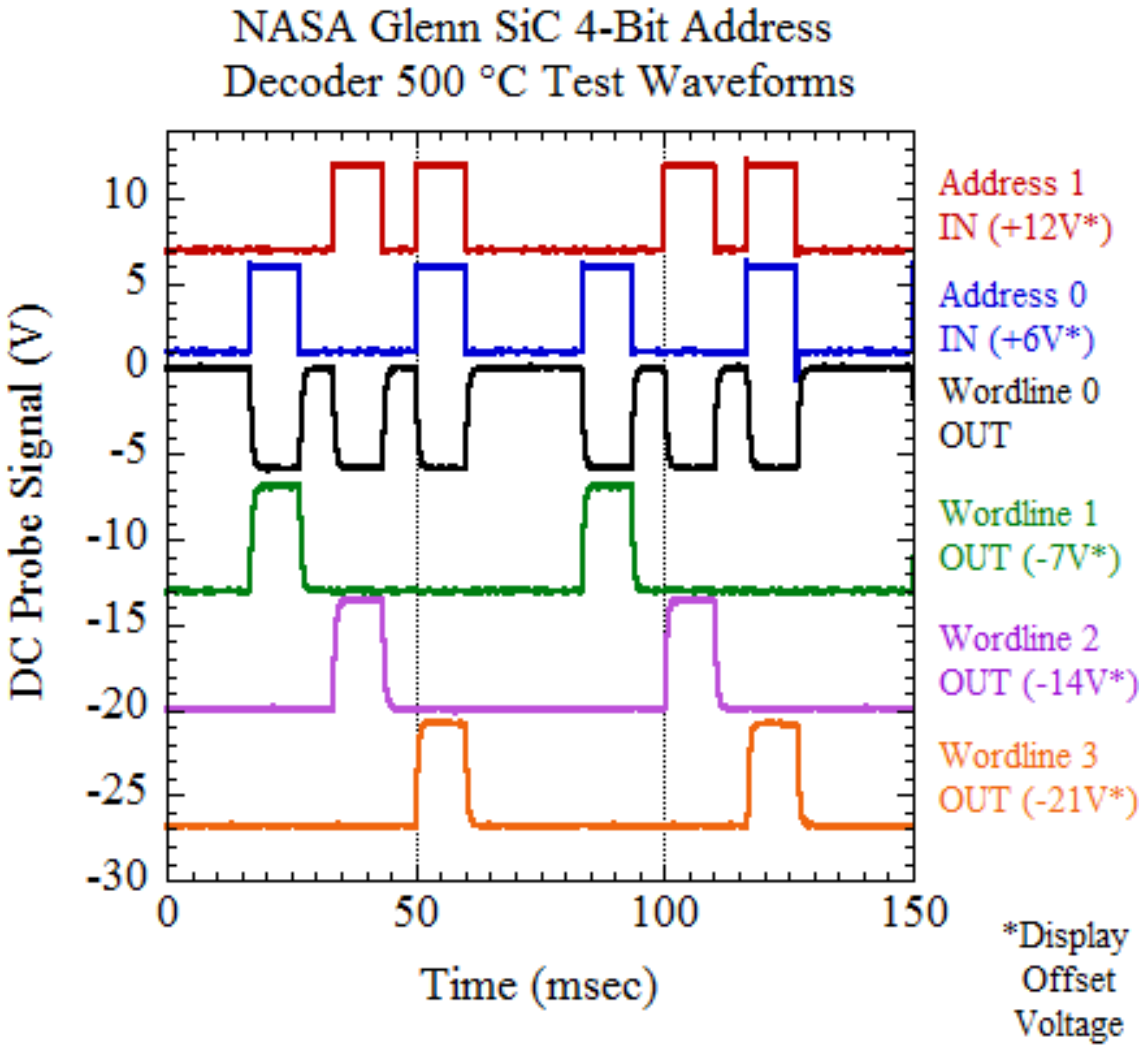
Traces enabling testing of RAM cell (3-3) without working sense amps.

4-Bit Address Decoder (24 Transistors)

RAM Cell (3-3) (6 Transistors/bit)

Address Decoder IC

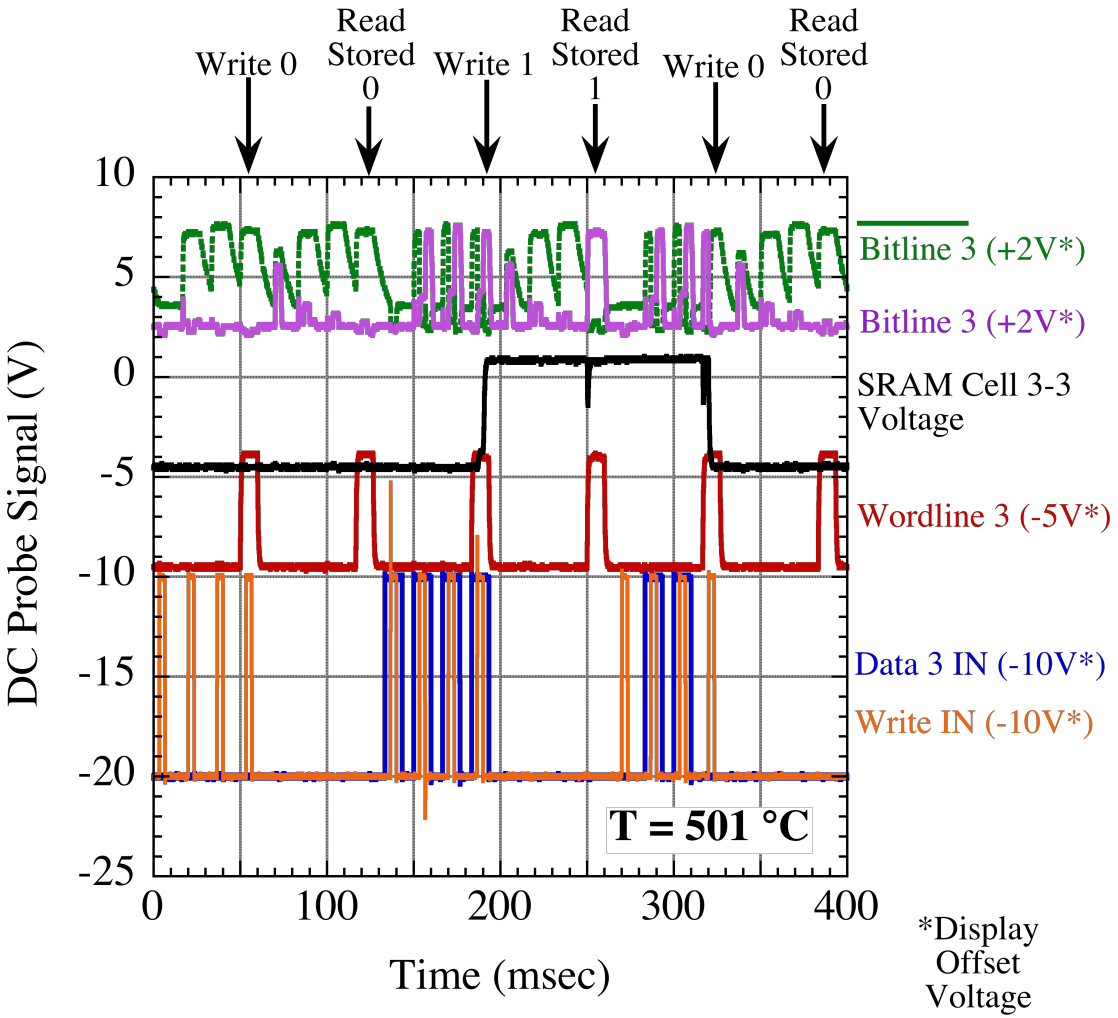
- 4-Bit Address Decoder operated for 120 hours at 500 °C.



-1 V to -5 V logic

RAM Cell 500 °C Demonstration

- One SRAM Cell (3-3) connected to bond pad for direct voltage measurement.
- Wordlines driven by Address Decoder IC
- Cell Read & Write only when addressed (by Wordline3).
- The SRAM cell operated at 500 °C for 9.5 hours.



~0 V to -5 V logic

Summary

- This work demonstrates the possibility of 4H-SiC JFET circuits with multilayer interconnects achieving prolonged operation at 500 °C in air ambient.
- Further process improvements and design rule changes will be needed to make larger-scale multilayer interconnect integrated circuits routinely function at these extreme temperatures for even longer time periods.
- Once larger-scale multilayer interconnect circuits have been fabricated with sufficient yield, more thorough reliability testing involving various temperatures, gas environments, and thermal cycling is planned.

Acknowledgements

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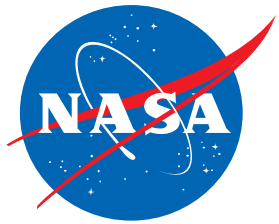
NASA

Integrated circuits in fabrication

Circuit	Inputs	Outputs	Transistors, I/O Pads	Comments
4-Bit A/D	Analog voltage signal, optional external clock, output type select	4 bit parallel digital latch, pulse width modulated (PWM)	203 JFETs, 23 I/Os	Internal ring-oscillator clock circuit
4X4 Bit Static RAM	Read, Write, Data Lines, Address Lines	4 bit parallel digital latch, pulse width modulated (PWM)	220 JFETs, 30 I/Os	Address decoder, sense amplifiers
Source Separation Sensor Signal Transmitter	Capacitive sensor	Frequency modulated with address code	301 JFETs, 20 I/Os	Each sensor signal is tagged with unique address code
Ring Oscillators	Capacitive sensors	Frequency modulated signals (up to 500 MHz)	10-12 JFETs, 6 I/Os	On-chip large transistors for power amplification
Binary Amplitude Modulation RF Transmitter	Low power binary signal	High-Power RF signal to antenna		Could connect with PWM from A/D
Op Amp, 2-Stage	Differential	Voltage gains to 50 w/ on-chip resistors	10 JFETs	For piezoresistive SiC pressure sensors
4-Bit D/A	4 digital	1 analog	20 JFETs	